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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,913	04/10/2001	A. Nicholas Sporck	P136-US	5250

27521 7590 04/13/2004

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,913	SPORCK ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-11,13-19,21,23-29,31,33-44 and 47-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-11,13-19,21,23-29,31,33-44 and 47-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3, 5-7, 19, 21, 23-25, 29, 37-39, 42, 47-50 and 56-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Khoury et al (6232669).

Regarding claim 1, Khoury et al disclose [see Fig. 2] a probe card assembly (combination of substrate handler 400 and interface assembly 140) for electrically communicating test data between a semiconductor test apparatus (test head 100) and a semiconductor device under test (wafer 300), the probe card assembly comprising a substrate (probe card 170) [see col. 2, lines 47-48] configured to electrically contact the semiconductor tester apparatus (100), a plurality of probes (probe contactors 190) configured to electrically contact the semiconductor device under test (300), the plurality of probes (190) located to a first side [referring to bottom side] of the substrate (170), a daughter card (interface assembly 140) located to a second side [referring to top side] of the substrate (170) and an electric circuit (combination of capacitors 193 and 195 as well as electric circuit of performance board 120 [not shown but see col. 1, lines 59-62]) at least

portion [see col. 1, lines 59-62] of which is disposed on said daughter card (140), wherein the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) receives as input test data received at said probe card assembly (140 and 400) from one of said tester apparatus (100) or said semiconductor device under test (wafer 300), enhances (filtering out noise or surge pulse) said test data [see col. 2, lines 47-61 and col. 3, lines 19-29] and outputs enhance test data.

Regarding claim 3, Khoury et al disclose the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) comprises an analog circuit element (capacitors 193 and 195).

Regarding claim 5, Khoury et al disclose the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) enhances said test data by customizing at least portion of the test data to test needs of said semiconductor device under test (300) [see col. 3, lines 9-40].

Regarding claim 6, Khoury et al disclose the test data comprises test signals generated by said semiconductor test apparatus (100) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) customizes at least portion of the test signals [see col. 3, lines 9-40].

Regarding claim 7, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) customizes at least portion of the response signals [see col. 3, lines 9-40].

Regarding claim 19, Khoury et al disclose [see Fig. 2] a method of making a probe card assembly (combination of substrate handler 400 and interface assembly 140), the method comprising providing a substrate (probe card 170) [see col. 2, lines 47-48] including a plurality of tester contacts (probe contacts 190), disposing a plurality of probes (190) to a first side [referring to bottom side] of the substrate (170) and configured to electrically contact a semiconductor device under test (wafer 300), and disposing a daughter card (interface assembly 140) to a second side [top side] of the substrate (20) providing an electric circuit (combination of capacitors 193 and 195 as well as electric circuit of performance board 120 [not shown but see col. 1, lines 59-62]) that receives as input test data received at said probe card assembly from one of said tester apparatus (test head 100) or said semiconductor device under test (300), enhances (filtering out noise or surge pulse) said test data [see col. 2, lines 47-61 and col. 3, lines 19-29] and outputs enhance test data and disposing at least portion of the electric circuit [electric circuit of performance board 120 (not shown but see col. 1, lines 59-62)] on said daughter card (140).

Regarding claim 21, Khoury et al disclose the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) comprises an analog circuit element (capacitors 193 and 195).

Regarding claim 23, Khoury et al disclose the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) enhances said test data by customizing at least portion of the test data to test needs of said semiconductor device under test (300) [see col. 3, lines 9-40].

Regarding claim 24, Khoury et al disclose the test data comprises test signals generated by said semiconductor test apparatus (100) and the electric circuit (capacitors 193 and 195 as

well as electric circuit of performance board 120) customizes at least portion of the test signals [see col. 3, lines 9-40].

Regarding claim 25, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) customizes at least portion of the response signals [see col. 3, lines 9-40].

Regarding claims 37-39 [see also Note below], Khoury et al disclose the probe card assembly (140 and 400) made using the process of claims 19-20 and 22.

[Note: "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)]

Regarding claim 42, Khoury et al disclose [see Fig. 2] a probe card assembly (combination of interface assmebly140 and substrate handler 400) comprising a printed circuit means (probe card 170) for electrically communicating with a semiconductor tester apparatus (test head100), contact means (probe contactors 190) configured to electrically communicating with semiconductor device under test (300), the contact means (30) being secured to a first side [bottom side] of the printed circuit means (170), electric circuit means (capacitors 193 and 195 as well as electric circuit of performance board 120) for enhances (filtering out noise or surge pulse) said test data [see col. 2, lines 47-61 and col. 3, lines 19-29] received at said probe card

assembly (140 and 400) from one of said semiconductor tester (100) or said semiconductor device under test (300) and daughter card means (interface assembly 140) for physically supporting at least portion of the electric circuit (electric circuit of performance board 120), the daughter card means (140) secured to a second side [top side] of the printed circuit means (170) wherein the daughter card (140) being substantially coplanar to the printed circuit means (170).

Regarding claim 47, Khoury et al disclose the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) enhances said test data by customizing at least portion of the test data to test needs of said semiconductor device under test (300) [see col. 3, lines 9-40].

Regarding claim 48, Khoury et al disclose the test data comprises test signals generated by said semiconductor test apparatus (100) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) customizes at least portion of the test signals [see col. 3, lines 9-40].

Regarding claim 49, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) customizes at least portion of the response signals [see col. 3, lines 9-40].

Regarding claim 50, Khoury et al disclose [see Fig. 2] a probe card assembly (combination of interface assembly 140 and substrate handler 400) for electrically communicating test data between a semiconductor test apparatus (test head 100) and a semiconductor device under test (wafer 300), the probe card assembly comprising a printed circuit board (probe card 170) con figured to electrically contact the semiconductor tester

apparatus (100), a plurality of probes (probe contactors 170) configured to electrically contact the semiconductor device under test (300), a daughter card (interface assembly 140) secured to the printed circuit board (170) and an electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) enhances (filtering out noise or surge pulse see col. 2, lines 47-61 and col. 3, lines 19-29) test capabilities of the semiconductor test apparatus (100) and is disposed on the daughter card (140).

Regarding claim 56, Khoury et al disclose the test data comprises test signals generated by the semiconductor tester apparatus (100) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) processes at least portion of the test signals [see col. 3, lines 9-40].

Regarding claim 57, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) processes at least portion of the response signals [see col. 3, lines 9-40].

Regarding claim 58, Khoury et al disclose said plurality of probes (190) are configured to contact a plurality of semiconductor devices under test (300), and said electric circuit capacitors 193 and 195 as well as electric circuit of performance board 120) enhances (filtering out noise or surge pulse see col. 2, lines 47-61 and col. 3, lines 19-29) said test data by receiving test signals from said tester apparatus (100) for testing a first number of semiconductor devices [located on wafer 300) and outputting to said probes test signals for testing a second number of semiconductor devices [located on wafer 300], wherein said second number is greater than said first number.

Regarding claim 59, Khoury et al disclose said daughter card (140) is substantially coplanar to said substrate (170) and there is a space between said daughter card (140) and said substrate (170) [via pogo pins 141].

Regarding claim 60, Khoury et al disclose said plurality of probes (190) are configured to contact a plurality of semiconductor devices under test (300), and said electric circuit capacitors 193 and 195 as well as electric circuit of performance board 120) enhances (filtering out noise or surge pulse see col. 2, lines 47-61 and col. 3, lines 19-29) said test data by receiving test signals from said tester apparatus (100) for testing a first number of semiconductor devices [located on wafer 300) and outputting to said probes test signals for testing a second number of semiconductor devices [located on wafer 300], wherein said second number is greater than said first number.

Regarding claim 61, Khoury et al disclose said daughter card (140) is substantially coplanar to said substrate (170) and there is a space between said daughter card (140) and said substrate (170) [via pogo pins 141].

Regarding claim 62, Khoury et al disclose said plurality of probes (190) are configured to contact a plurality of semiconductor devices under test (300), and said electric circuit capacitors 193 and 195 as well as electric circuit of performance board 120) enhances (filtering out noise or surge pulse see col. 2, lines 47-61 and col. 3, lines 19-29) said test data by receiving test signals from said tester apparatus (100) for testing a first number of semiconductor devices [located on wafer 300) and outputting to said probes test signals for testing a second number of semiconductor devices [located on wafer 300], wherein said second number is greater than said first number.

Regarding claim 63, Khoury et al disclose said daughter card means (140) is substantially coplanar to said contact means (170).

Regarding claim 64, Khoury et al disclose said plurality of probes (190) are configured to contact a plurality of semiconductor devices under test (300), and said electric circuit capacitors 193 and 195 as well as electric circuit of performance board 120) enhances (filtering out noise or surge pulse see col. 2, lines 47-61 and col. 3, lines 19-29) said test data by receiving test signals from said tester apparatus (100) for testing a first number of semiconductor devices [located on wafer 300) and outputting to said probes test signals for testing a second number of semiconductor devices [located on wafer 300], wherein said second number is greater than said first number.

Regarding claim 65, Khoury et al disclose said daughter card (140) is substantially coplanar to said substrate (170) and there is a space between said daughter card (140) and said substrate (170) [via pogo pins 141].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 8-11, 13-18, 26-29, 31, 33-36, 40-41, 43-44 and 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Khoury et al (6232669).

Regarding claims 8-9, 16, 18, 26-27, 34, 36, and 51-55, Khoury et al disclose [see Fig. 2] a daughter card (interface assembly 140) located to a second side [referring to top side] of the substrate (170) wherein the daughter card (140) being substantially coplanar to the substrate (170). However, they do not disclose a plurality of daughter cards as claimed. It is well known to have more than one daughter card where needed (see MPEP 2144.04 *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have more than one daughter card since the plurality of cards, which is mere duplication of a single daughter card, would provide support to selective manner to each individual user that will like to duplicate the function of processing signals passing between a semiconductor tester and a semiconductor device under test.

Regarding claims 10, 17, 28, and 35, Khoury et al disclose at least portion of the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) is disposed on the daughter card (140).

Regarding claims 11, 29, Khoury et al disclose the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) comprises an analog circuit element (capacitors 193 and 195).

Regarding claims 13, 31, Khoury et al disclose the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) enhances said test data by customizing at least portion of the test data to test needs of said semiconductor device under test (300) [see col. 3, lines 9-40].

Regarding claims 14, 32, Khoury et al disclose the test data comprises test signals generated by said semiconductor test apparatus (100) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) customizes at least portion of the test signals [see col. 3, lines 9-40].

Regarding claims 15, 33, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (capacitors 193 and 195 as well as electric circuit of performance board 120) customizes at least portion of the response signals [see col. 3, lines 9-40].

Regarding claims 40-41 [see Note below], Khoury et al disclose the probe card assembly (140 and 400) made using the process of claims 26 and 30.

[Note: "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)]

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kwon et al (5070297), D'Souza (5323107), Nakajima et al (5642056), Aldaz et al (6476626), Cheng et al (6621710), Zhou et al (6677771) disclose a method and apparatus for a probe card assembly.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (517) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
April 1, 2004

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